Remarks

After entry of this amendment, claims 34-54 should be pending. Claim 36 has been amended. New claims 41-54 have been added.

I. Claim Objections

Claim 36 was objected-to because of a misspelled word. Applicants have amended claim 36 to correct this error.

II. Claim Rejections - 35 U.S.C. § 102

Claims 34-40 were rejected under 35 U.S.C. § 102 as allegedly being anticipated by Published U.S. Patent Application No. 2001/0002056 (Manning). Applicants traverse this rejection and respectfully request that it be withdrawn.

Applicants' claim 34 includes "forming a hard mask over the insulating layer." The Examiner cites paragraph 31 in Manning as implying this limitation. Manning, however, does not disclose a hard mask. Paragraph 31 in Manning simply states that "[a]n anisotropic step is then performed to remove the deposited oxide from the horizontal surfaces." Paragraph 31, lines 3-4. This implies the use of a conventional dry etch process. Such a process would include coating the oxide with a layer of photoresist, patterning the photoresist and then performing a plasma etch to selectively remove the portions of the oxide layer not covered by the photoresist. The patterned photoresist then would be removed, e.g. by ashing or stripping, before any subsequent processing. In contrast, the patterned hard mask described in Applicants' claim 34 remains intact while the spacers are deposited. Thereafter, the patterned hard mask functions as an etch stop preserving the walls of the buried bit line trenches while the spacers are recessed and the portions of the insulating layer within the cell contact trenches are removed. Applicants' Figures 12-14. A person of ordinary skill in the art would not equate a hard mask, as recited in Applicants' claim 34, with a photoresist layer. Furthermore, since Manning does not disclose the use of a hard mask, Manning also does not disclose "patterning the hard mask to define cell contacts above the active areas and buried bit lines between the cell contacts," as recited in Applicants' claim 34.

With respect to Applicants' claims 34-36, the Examiner cites Figure 9 in Manning as showing the limitation of "removing a portion of the insulating layer to form cell contact trenches and buried bit line trenches." Manning's Figure 9, however, shows no buried bit line trenches. In fact, none of Manning's device illustrations (Figures 5-13) show buried bit line trenches or buried bit

lines, such as "buried bit lines between the cell contacts," as recited in Applicants' claims 34 and 35, or "buried bit lines above shallow trenches of the transistors," as recited in Applicants' claim 36. In Manning, the portion of the second conductor 237 that is deposited over active area 110 does not appear to function as a bit line. While bit lines often contact the gates of transistors on the periphery of a memory device, they typically do not contact the gates of the transistors that form the actual memory cells. As shown in Manning's Figure 5, the second conductor 237 contacts transistor gate 114 at cell contact 126. Thus, the second conductor 237 probably is a local interconnect, although this cannot be verified by Manning's disclosure.

Applicants' claims 34-36 also recite limitations relating to the deposition of spacers into the buried bit line trenches. The Examiner cites element 232 in Manning's Figure 10 as a spacer, but this element has no resemblance to the spacers described in Applicants' disclosure. Manning's element 232 is a dielectric layer that isolates the second conductor. For the sake of argument, even if element 232 is considered to be a spacer, it still is not deposited into a buried bit line trench. As mentioned above, the trench above the second conductor does not serve as a bit line trench. Paragraph 27 in Manning implies that the region adjacent to contact area 132 in Figure 5 may be a bit line trench, but this feature is far removed from element 232 and there is no indication that it serves as a *buried* bit line trench.

Manning also does not disclose "recess[ing] the spacers within the buried bit lines," as recited in Applicants' claims 34 and 35, or "partially removing the spacers within the buried bit lines," as recited in Applicants' claim 36. In Manning, the size and shape of dielectric layer 232 over active area 110 never changes. Paragraph 33 in Manning, which was cited by the Examiner, merely describes how dielectric layer 232 is patterned to expose the active areas and the poly one layer. Since Manning does not disclose spacers, let alone recessing or partially removing spacers, Manning cannot not disclose "removing the dielectric material and portions of the insulating layer within the cell contact trenches to expose the active areas underlying the cell contacts while recessing [or partially removing] the spacers within the buried bit lines," as recited in Applicants' claims 35 and 36, respectively.

Applicants' claim 37 depends from claim 36 and is allowable for the reasons stated for claim 36. Claim 37 is further allowable in view of the patentable combination of features it recites. Claim 37 recites the method of claim 36, wherein the spacers comprise TEOS or silicon dioxide. Although element 232 in Manning can be made of TEOS or silicon dioxide, it is not a spacer.

Applicants' claims 38, 39 and 40 recite semiconductor devices made according to the processes of claims 34, 35 and 36, respectively. Since Manning does not disclose the processes recited in Applicants' claims 34, 35 and 36, Manning also does not disclose devices made according to these processes. Moreover, the devices described in Manning do not include one or more features that would be found in the devices made according to the processes recited in Applicants' claims 34, 35 and 36. For example, devices made according to the processes recited in Applicants' claims 34, 35 and 36 would comprise buried bit lines, which are not found in the devices disclosed by Manning.

III. New Claims

Applicants have added claims 41-54. Support for new claims 41 and 46 can be found, for example, in the specification at page 12, lines 1-4. Support for new claims 42, 47 and 51 can be found, for example, in the specification at page 11, line 10. Support for new claims 43, 48 and 52 can be found, for example, in the specification at page 11, lines 12-13. Support for new claims 44, 49 and 53 can be found, for example, in the specification at page 11, lines 13-14. Support for new claims 45, 50 and 54 can be found, for example, in the specification at page 11, lines 13-15.

IV. Conclusion

For the above set out reasons, it is respectfully submitted that all of the claims now in the application define over the cited prior art, are neither anticipated nor made obvious by the prior art, and should be allowable. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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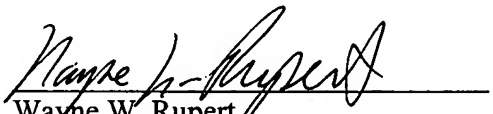
By 
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